Isolated Autonomous Capacitive Power Supplies to Trigger Floating Semiconductors in a Marx Generator

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Abstract - This paper reports the development of isolated autonomous capacitive power supplies to charge each drive circuit of the high voltage floating semiconductor stage in a solid-state Marx Generator. The circuit takes advantage of an auxiliary capacitor, charged in series with the main energy storage capacitor in each Marx generator stage, to supply the optic-fibre isolated gate drive circuit of the solid state switches. Laplace domain circuit analysis is made to determine the values of these capacitors and to obtain the desired voltages, with low ripple, for the required load. A laboratory prototype with three stages, 3 kW peak power, of this all silicon Marx generator circuit, with optic-fibre isolated triggering signals and autonomous capacitor isolated charging power supplies was built using 1200 V IGBTs and diodes, operating with 1000 V d-c input voltage and 10 kHz frequency, giving 3 kV and 10 μs pulse with, approximately, 15 V isolated autonomous power supplies in each stage.

I. INTRODUCTION

Today, rectangular high-voltage and high-frequency electrical pulses find many applications in industry. Some typical applications evolve in surface treatment techniques [1], food sterilisation [2] and waste treatment [3].

The high-voltage pulses can be generated using several known techniques [4-6], such as the widely used Marx-bank generator concept [5]. This approach has been used through the years, with continuous technological upgrades to increase the life-time and obtain higher pulse repetition rates. Recent developments, using only solid-state switches in the Marx topology, have contributed to improve the circuit performance [7 - 11].

Fig. 1 shows one example of an all-solid-state electronic Marx generator (EMG) that delivers negative high-voltage and high-frequency pulses to a load. This circuit substitutes all the dissipative elements of the traditional circuit, but the energy storage capacitors, by rearranged semiconductors, as described in [10].

Each stage, of Fig. 1 circuit, consists of an energy storing capacitor C_{pi}, a diode D_{ci} and two IGBTs (T_{ci} and T_{di}), for controlling the supply and pulse periods, where the subscript $i \in \{1, 2, \ldots, n-1, n\}$ [10].

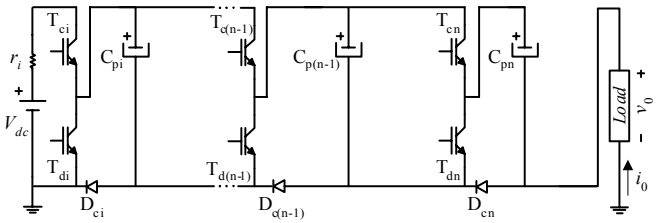


Fig. 1. Basic topology of the EMG circuit, with n stages, for negative output pulses in the load [10].

Similar to other semiconductor stack associations used to achieve the desire high-voltage, the semiconductors of the Marx generator topology, Fig. 1, are located at different high-voltage potentials, which are floating in relation to ground potencial, requiring galvanically isolated gate drive signals.

Several solutions are possible to supply the drive circuits of each Marx stage. The simplest solution would be the use of batteries. Yet, this solution is not sustainable. The use of transformer isolated power supplies can be cumbersome. Auxiliary isolated power supply with diode string connected to each stage was also considered [9].

The semiconductor gate drive circuits, with galvanic insulation, can be generically classified depending on the insulation coupling environment used for transmitting the drive signals. First, considering magnetic coupling, if pulse transformers are used, it is possible to transmit both the drive signal and the necessary power to switch directly the semiconductors. Hence, to drive series stacked solid-state switches, distributed magnetic structures, consisting of a number of pulse transformers with primary windings in series and independent isolated secondary windings, are usually needed [12-13].

Second, considering electrical coupling, transformerless capacitive coupling structures are used to drive series connection of semiconductors. The operation of these circuits relies on a voltage division among the input capacitance of the devices [14-15].

Third, considering optic coupling, opto-couplers or optic-fibres are, also, used to galvanic isolate gate drive signals, to trigger semiconductors placed at high-voltage potential. However, this method requires isolated power supplies to further process the transmitted gate signal and supply the gate drive circuit of the semiconductors [9-10].

Taken into account the circuit topology of Fig. 1 and the above description, optic-fibres were used for triggering. In addition of being immune to EMI (Electromagnetic Interference), this solution as the advantage of further reducing stray capacitances to ground and spacing.

Concerning the isolated charging power supply, the topology shown in Fig. 1 enables the use of typical half-bridge semiconductor structures, with alternate semiconductor switching, as describe in [10], which allows bootstrap operation, as seen in Fig. 2. Thus, it is only necessary to supply the bottom semiconductor of each half-bridge structure.

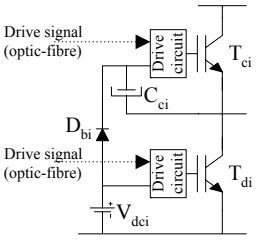


Fig. 2. Half-bridge semiconductor structure, with alternate semiconductor switching, which allow bootstrap operation. [10].

The concept developed and described in this work, for supplying each gate drive circuit, takes advantage of the main high voltage energy storage capacitor, in each stage, to supply an auxiliary capacitor in series. This concept determines that each stage is independent and autonomous from the others and from the exterior, depending only on the energy stored in the auxiliary capacitor. Laplace domain circuit analysis is here used to determine the values of the main (C_{pi}) and auxiliary (C_{si}) capacitors, shown in Fig. 3, to obtain the desired voltages, with low ripple, for the required load.

A laboratory prototype with three stages, 3 kW peak, of this all silicon Marx generator circuit, was constructed using 1200 V IGBTs and diodes, operating with 1000 V d-c input voltage and 10 kHz repetition frequency. First experimental results show 3 kV and 10 μs pulses, obtained from isolated autonomous power supplies, with around 15 V, that supplied optical fibre isolated gate circuits.

II. CIRCUIT TOPOLOGY

The basic topology of the Electronic Marx Generator (EMG), with n stages, able to deliver negative high-voltage output pulses, is presented in Fig. 1 (Patent PT103150), as described in [10].

Fig. 3 shows the Marx generator topology of Fig. 1 with the isolated autonomous powers supplies for charging the floating semiconductors in each stage. Considering the circuit shown in Fig. 3, C_{si} represents the gate charging auxiliary capacitor, D_{fi} and D_{ei} auxiliary diodes and R_{si} represents the equivalent load of the two triggering circuits in each stage, shown in Fig. 2.

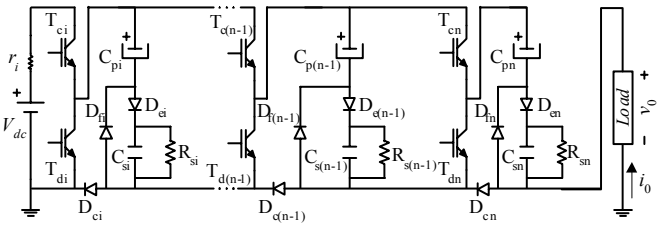


Fig. 3. Basic topology of the EMG circuit with auxiliary capacitor, with n stages, for negative output pulses to the load.

Fig. 3 circuit operation can be understood, considering only two different operating modes. In the first operating mode, switches T_{ci} and T_{di} are, respectively, on and off, and Fig. 3 circuit assumes the topologies shown in Fig. 4. During this period, capacitors C_{pi} and C_{si} are charged from the dc power supply, V_{dc}, through T_{ci} and D_{ci} and D_{ei} as shown in Fig. 6.

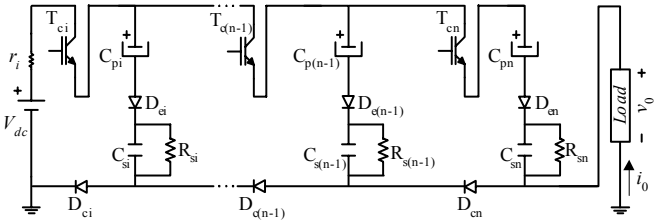


Fig. 4. Capacitors charging operation mode of the EMG with auxiliary capacitor in Fig. 3.

In the second operating mode, pulse mode, switches T_{ci} and T_{di} are, respectively, off and on, and Fig. 3 circuit assumes the topologies shown in Fig. 5. During this period, capacitors C_{pi} and C_{si} are partially discharged as shown in Fig. 6.

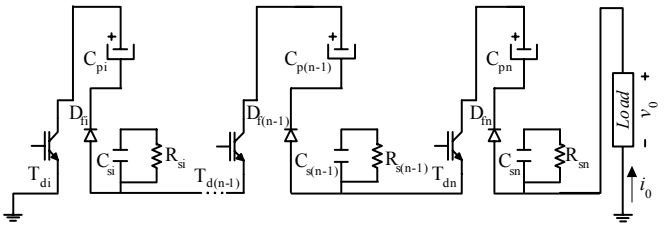


Fig. 5. Pulse operation mode of the EMG with auxiliary capacitor in Fig. 3.

During the pulse mode, capacitors C_{pi} are connected in series through D_{fi} and the voltage applied to the load is, approximately,

$$v_0 = -n(V_{dc} - V_{Cs}), \tag{1}$$

as capacitors C_{pi} are charged with $V_{dc} - V_{Cs}$, as shown in Fig. 6. Considering [10], this value depends: *i*) on the characteristics of the components; *ii*) on the operating frequency; *iii*) on the capacitors charge time, t_c, being much longer the discharge time, t_d, meaning that T_{ci} and T_{di} operate, respectively, with a

long ($\delta_c=t_c/T$) and short ($\delta_d=t_d/T$) switching duty cycle, as shown in Fig. 6.

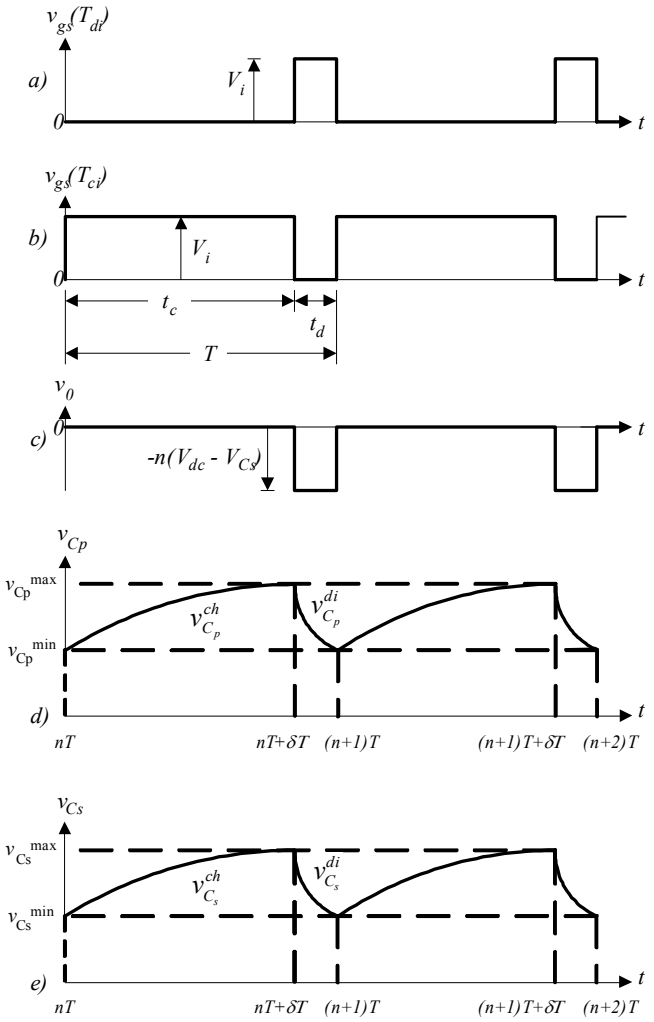


Fig. 6. Theoretical waveforms for the operation of the EMG of Fig. 3, considering a resistive load: a) drive signal of semiconductors T_{di}; b) drive signal of semiconductors T_{ci}; c) load voltage, v_0; d) capacitor C_p voltage, v_{Cp}; e) capacitor C_s voltage, v_{Cs}.

The values for the energy storage (main) and auxiliary capacitors in order to obtain the desire voltages, in the EMG of Fig. 3, can be determined by modelling the voltage time evolution in these capacitors, during the charge phase and pulse mode operation.

Fig. 6 d) and e) shows, respectively, the theoretical evolution of the main and auxiliary capacitor voltage C_{pi} and C_{si} during the supply time, v_{Cpi}^{ch}, v_{Csi}^{ch} and discharge time v_{Cpi}^{di}, v_{Csi}^{di}. These voltages can be calculated, assuming that the circuit parasitic capacitances, as well as the voltage drop on the diodes are negligible. Consequently, the circuit becomes linear and the analysis in the Laplace domain is possible. First, considering the charging operation mode, Fig. 7 shows one stage of Fig. 4 circuit in the Laplace domain.

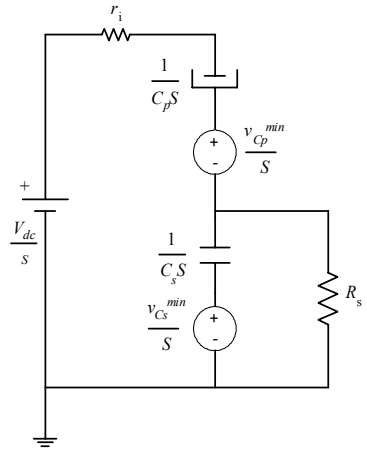


Fig. 7. Fig. 4 capacitors charging operation mode in Laplace domain.

Analysing Fig. 6, between nT and $nT+\delta T$, capacitors C_p and C_s at time nT^- are charged with $v_{C_p}^{\min}$ and $v_{C_s}^{\min}$, respectively. Then, network analysis in Fig. 7 circuit, results in,

$$\begin{cases} -\dfrac{V_{dc}}{S}+r_iI_1+\dfrac{1}{C_pS}I_1+\dfrac{v_{C_p}^{\min}}{S}+\dfrac{1}{C_sS}(I_1-I_2)+\dfrac{v_{C_s}^{\min}}{S}=0 \\ -\dfrac{v_{C_s}^{\min}}{S}+\dfrac{1}{C_sS}(I_2-I_1)+R_sI_2=0 \end{cases} \quad (2)$$

Solving (2), the voltages of the both capacitors during the charging period are,

$$v_{Cp}^{ch}=ae^{\omega_1(t-nT)}+be^{\omega_2(t-nT)}+v_{dc}\,, \quad (3)$$

$$v_{Cs}^{ch}=f^{\omega_1(t-nT)}+ge^{\omega_2(t-nT)}\,, \quad (4)$$

where the coefficients ω_1, ω_2, a, b, f and g are, respectively, given by,

$$\omega_1=-\frac{R_sC_s+C_p(R_s+r_i)}{2r_iR_sC_pC_s}+\sqrt{\frac{\left[R_sC_s+C_p(R_s+r_i)\right]^2}{(2r_iR_sC_pC_s)^2}-\frac{1}{r_iR_sC_pC_s}}\,, \quad (5)$$

$$\omega_2=-\frac{R_sC_s+C_p(R_s+r_i)}{2r_iR_sC_pC_s}-\sqrt{\frac{\left[R_sC_s+C_p(R_s+r_i)\right]^2}{(2r_iR_sC_pC_s)^2}-\frac{1}{r_iR_sC_pC_s}}\,, \quad (6)$$

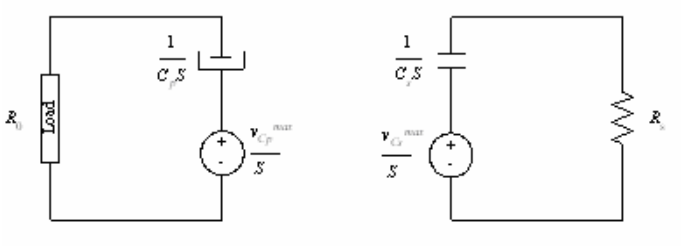
$$a=\frac{R_sC_s\omega_1\left(V_{dc}-v_{Cp}^{\min}-v_{Cs}^{\min}\right)+V_{dc}-v_{Cp}^{\min}}{r_iR_sC_sC_p\omega_1(\omega_1-\omega_2)}\,, \quad (7)$$

$$b=\frac{R_sC_s\omega_2\left(V_{dc}-v_{Cp}^{\min}-v_{Cs}^{\min}\right)+V_{dc}-v_{Cp}^{\min}}{r_iR_sC_sC_p\omega_2(\omega_2-\omega_1)}\,, \quad (8)$$

$$f = \frac{R_s C_p \omega_1 \left(V_{dc} - v_{Cp}^{\min} - v_{Cs}^{\min} - \frac{r_i}{R_s} v_{Cs}^{\min} \right) - v_{Cs}^{\min}}{r_i R_s C_s C_p \omega_1 (\omega_1 - \omega_2)}, \quad (9)$$

$$g = \frac{R_s C_p \omega_2 \left(V_{dc} - v_{Cp}^{\min} - v_{Cs}^{\min} - \frac{r_i}{R_s} v_{Cs}^{\min} \right) - v_{Cs}^{\min}}{r_i R_s C_s C_p \omega_2 (\omega_2 - \omega_1)}. \quad (10)$$

Between $nT+\delta T$ and $(n+1)T$, considering the pulse operation mode, Fig. 8 shows the equivalent of Fig. 5 circuit in the Laplace domain.



a) b)

Fig. 8. Fig. 5 capacitors discharge mode in Laplace domain: a) C_p discharge mode to the load R_0; b) C_s dissupply mode to the load R_s.

Analysing Fig. 6, between $nT+\delta T$ and $(n+1)T$, the capacitors C_p and C_s in instant $nT+\delta T^-$ are found charged with $v_{C_p}^{\max}$ and $v_{C_s}^{\max}$ respectively. Then, network analysis in both circuits of the Fig. 8, results in,

$$I_{a)} = \left(\frac{v_{Cp}^{\max}}{R_0} \right) \Big/ \left(S + \frac{1}{R_0 C_p} \right), \quad (11)$$

$$I_{b)} = v_{Cs}^{\max} \Big/ \left[R_s \left(S + \frac{1}{R_s C_s} \right) \right], \quad (12)$$

where $I_{a)}$ and $I_{b)}$ represent, respectively, Fig. 8 a) and b) currents. From (11) and (12) results the capacitors C_p and C_s voltages in Laplace domain, respectively,

$$V_{Cp}^{di} = \left(-I_{a)} \right) / \left(C_p S \right) + v_{Cp}^{\max} / S, \quad (13)$$

$$V_{Cs}^{di} = \left(-I \right) / \left(C_s S \right) + v_{Cs}^{\max} / S. \quad (14)$$

Appling the Inverse Laplace Transform to (13) and (14), result, the voltages of the both capacitors during the pulse period,

$$v_{Cp}^{di} = v_{Cp}^{\max} e^{-\frac{1}{R_0 Cp}[t-(nT+\delta T)]}, \quad (15)$$

$$v_{Cs}^{di} = v_{Cs}^{\max} e^{-\frac{1}{R_s C_s}[t-(nT+\delta T)]}. \quad (16)$$

The values of capacitors C_p and C_s can be determined from Fig. 6 at times nT^- and $(n+1)T^-$, assuming equal the voltages in the capacitors at the specified times. The last condition is expressed by,

$$v_{Cp}^{ch}\left(t = nT^-\right) = v_{Cp}^{di}\left[t = (n+1)T^-\right], \quad (17)$$

$$v_{Cs}^{ch}\left(t = nT^-\right) = v_{Cs}^{di}\left[t = (n+1)T^-\right], \quad (18)$$

which can be written as,

$$v_{Cp}^{ch}\left(t = nT^-\right) = v_{Cp}^{\min} = v_{Cp}^{di}\left[t = (n+1)T^-\right] = v_{Cp}^{\max} e^{-\frac{1}{R_0 C_p}[(n+1)T-(nT+\delta T)]}, \quad (19)$$

$$v_{Cs}^{ch}\left(t = nT^-\right) = v_{Cs}^{\min} = v_{Cs}^{di}\left[t = (n+1)T^-\right] = v_{Cs}^{\max} e^{-\frac{1}{R_s C_s}[(n+1)T-(nT+\delta T)]}, \quad (20)$$

Solving (19) and (20) results in, the values of capacitors C_p and C_s, respectively,

$$C_p = \frac{-(T-\delta T) / \ln\left(v_{Cp}^{\min} / v_{Cp}^{\max} \right)}{R_0}, \quad (21)$$

$$C_s = \frac{-(T-\delta T) / \ln\left(v_{Cs}^{\min} / v_{Cs}^{\max} \right)}{R_s}, \quad (22)$$

which are calculated to obtain the correct auxiliary voltage around 15 V, with low ripple, for charging the gate drive circuits of each EMG stage.

III. Results

A laboratory prototype of the EMG, circuit of Fig. 3, with autonomous power supplies for charging each drive circuit of the high voltage floating semiconductor stage, was built. The circuit with three stages was built using 1200 V IGBTs and diodes, operating with V_{dc}=1000 V, 10% duty cycle and 10 kHz repetition rate.

The theoretical capacitors values, from (21) and (22), considering an average voltage of 985 V for C_{pi} and 15 V for C_{pi}, and a 0.2 % ripple for both, were, respectively, 5 μF for C_{pi} and 10μF for C_{si}. For the C_{si} calculation, it was assume that each trigger circuit of the EMG has a load of 50 mA (i.e. each half-bridge stage has a load of 100 mA, Fig. 2).

The experimental capacitors values used in each stage were, 4.5 μF for C_{pi} and 10μF for C_{si}.

Fig. 9 shows the pulse, v_0, and pulse current, i_0, for a resistive load.

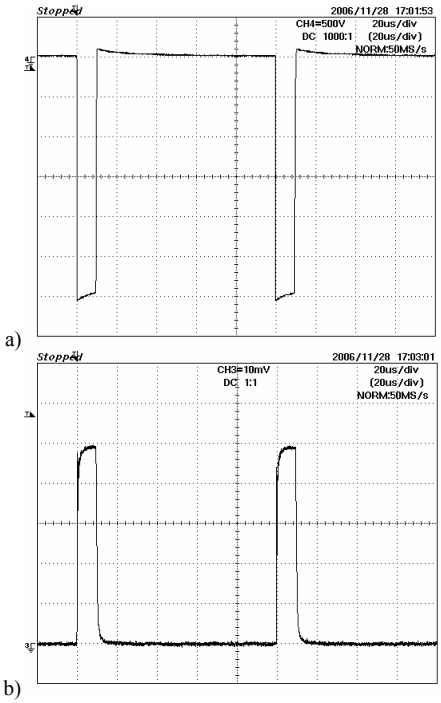


Fig. 9. Experimental results for the EMG of Fig.3, horizontal scale 20 (μs/div): a) Voltage pulse, v_0, 500 (V/div); b) Current, i_0, 0.2 (A/div).

The voltage pulse, in Fig. 9 a), exhibit an almost rectangular shape with - 3 kV amplitude and 10 μs width, giving 1 A, into a resistive load, Fig. 9 b).

Fig. 10 shows the capacitor v_{Cs1} voltage for the EMG circuit of Fig. 3 for the first stage.

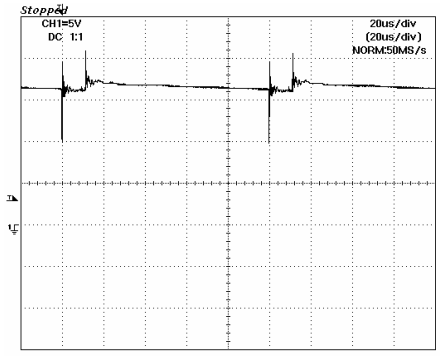


Fig. 10. Experimental results for the EMG of Fig.3, horizontal scale 20 (μs/div), capacitor C_{s1} voltage 5 (V/div).

The capacitor C_{s1} voltage has an average value of about 17 V, in Fig. 10. Measuring the voltage of stage two and three it yielded, respectively, an average voltage of 16 V and 15 V, respectively, for stage two and three.

Fig. 11 shows the simulated capacitor v_{Cs} voltage for each stage of the EMG circuit of Fig. 3, considering (3) – (4) and (15) – (16).

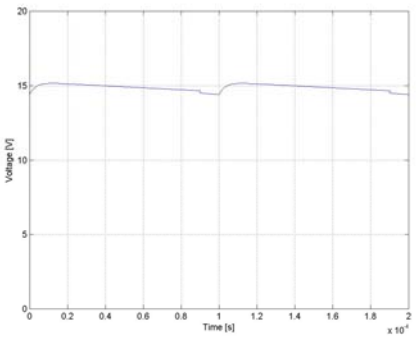


Fig. 11. Simulation result for the Fig.3 EMG with auxiliary capacitor Cs_1 voltage, v_{Cs1}, vertical scale 5 (V/div) and horizontal scale 20 (μs/div).

In Fig. 11 the auxiliary capacitors average voltage of are near 17 V, 17 V and 15 V, respectively, for the auxiliary capacitors in the first, second and third generator stage.

Comparing the simulated and experimental values for the auxiliary capacitors used to supply each EMG stage of Fig. 3, it results that the values are in good agreement, being the differences due to the simplifications used in the simulation.

IV. CONCLUSIONS

A capacitor coupled supply circuit for the gate drives of solid-state Marx Generator has been proposed. The topology needs no extra switches and has the advantage of keeping each stage independent and autonomous from the others and from the exterior, depending only on the energy stored in one auxiliary capacitor, where the main high voltage energy storage capacitor, in each stage, is used to supply an auxiliary capacitor in series and the isolation is also guarantied.

Laplace domain circuit analysis was used to determine the values of the main (C_{pi}) and auxiliary (C_{si}) capacitors to obtain the desire voltages, with low ripple, for the required gate drive requirements.

A laboratory prototype with three stages, 3 kW peak power, of this all silicon Marx generator circuit, was built using 1200 V IGBTs and diodes, operating with 1000 V d-c input voltage and 10 kHz repetition frequency. First experimental results show 3 kV and 10 μs pulses, obtain from isolated autonomous power supplies, with around 15 V, that supply optical fibre coupling gate circuits. Experimental and simulation results for the supply voltage are in good agreement.

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