Low-voltage semiconductor topology for kV pulse generation using a leakage flux corrected step-up transformer

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Abstract - This paper introduces a new circuit to obtain high voltage (kV) pulsed power supplies suitable for plasma ion implantation. Using a step-up transformer with a leakage flux reduction winding, and taking advantage of the low duty ratio required, 800V semiconductor switches can be used to obtain 5kV 10kHz pulses. Theoretical and experimental results are presented.

I. INTRODUCTION

Today, high voltage pulses (>10kV) have a broad spectrum of applications. Namely, X-rays tubes for medical and industrial use, gas lasers for plasma technology, plasma immersion ion implantation (PIII). This paper is concerned with PIII, a versatile new method for implanting ions, which can be used to modify the surface properties of materials and to obtain new compounds. With this technique, the sample is immersed in a plasma and short negative high voltage pulses are applied to it, resulting in the acceleration of the ions into the surface of the sample [1].

These high voltage pulses can be generated by different technologies. The most widely used combines a high voltage power supply and a vacuum or plasma switch to modulate the voltage on and off. Modern devices are capable of switching power in the range megawatts. A recent possibility is the use of semiconductor switches. Semiconductor based high voltage pulse supply (HVPS) have the great advantage of eliminating the need for large auxiliary power supplies and the very low voltage drop of semiconductors results in very efficient based semiconductor HVPS [2].

There are two major issues facing semiconductor based HVPS design. One is that the voltage rating of semiconductors presently doesn't exceed a few kilovolts. To achieve the high voltage pulsing needs characteristics (>10kV), either large series combinations of switches that have to be driven synchronously or resonant circuit associations must be used [3]. Operating cascaded stacks of semiconductors introduces the complexity of floating multiple drivers to high voltage. The second issue is that semiconductors are susceptible to damage from high voltage transients commonly caused by arcs or fault conditions. Snubber and clamp protection circuits can solve this problem, but care must be taken to avoid large snubber losses.

Step-up transformers can be applied to further increase the output voltage pulses. However, the usually large number of turns in the secondary winding in addition with the insulation gap between windings and layers increase the value of the equivalent parasitic elements (leakage inductance and inter-winding capacitance), which extend the pulse rise time and cause overshoots and oscillations.

This work presents a new topology to generate high voltage pulses based on a step-up transformer, fitted with an auxiliary winding to reduce the transformer equivalent leakage inductance. The topology enables the use of low voltage semiconductor devices in the transformer secondary. This is accomplished, considering the low duty ratio operation required together with a constant voltage flux reset clamp circuit of the transformer. Theoretical aspects about the operation of the auxiliary winding are presented and experimentally evaluated. To reduce the voltage overshoot caused by the auxiliary winding, an auxiliary semiconductor to switch this winding on or off is also proposed and tested.

II. CIRCUIT THEORY

A. Topology

The simplified circuit diagram used to obtain negative high voltage pulses is shown in Fig 1, where the reset of the step-up transformer is accomplished during the S switch *off* interval, using a resistor-capacitor-diode (RCD_2) clamp reset circuit, according to [4].

Applying volt-second balance on the primary of the transformer, the voltage across the clamp capacitor, V_c, which is assumed constant if C is sufficiently large, should satisfy,

$$\frac{V_c}{V_i} = \frac{t_{on}}{\Delta_1 T} = \frac{D}{\Delta_1} \tag{1}$$

where $\Delta_1 T = \tau$, shown in Fig. 1, is the transformer resetting time, and $D = t_{on}/T$ is the circuit switching duty ratio. When the S switch is *on* for a time t_{on}, diode D_1 conducts and the

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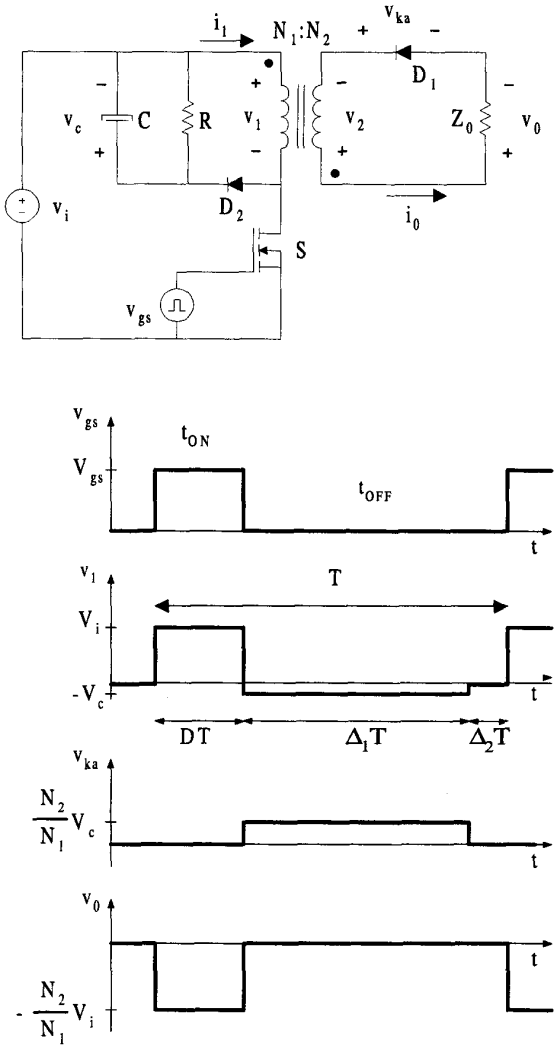

Fig. 1. Simplified circuit diagram (top). Circuit key waveforms (bottom).

voltage across the load, Z_0, is given by (2), where N_2/N_1 is the inverse of the turns ratio.

$$V_0 = -\frac{N_2}{N_1} V_i \tag{2}$$

When the S switch is *off* for a time $t_{off}=(\Delta_1+\Delta_2)T$, the voltage across the load is zero. During this time the reverse voltage of diode D_1 is,

$$V_{ka} = \frac{N_2}{N_1} V_c = \frac{N_2}{N_1} V_i \frac{D}{\Delta_1} \tag{3}$$

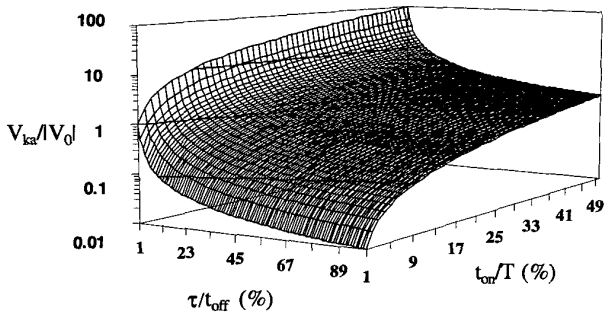

Fig. 2. Ratio of the reverse voltage, V_{ka}, of diode D_1 to the absolute value of the output voltage, $|V_0|$, as a function of the switching duty ratio (t_{on}/T), and the ratio of the transformer resetting time to the switching off time (τ/t_{off}).

If the ratio of the transformer resetting time, τ/t_{off}, to the S switch *off* time is taken into account (considering the absolute value of the output voltage $|V_0|$), (3) becomes,

$$\frac{V_{ka}}{|V_0|} = \left(\frac{D}{\frac{\tau}{t_{off}}(1-D)} \right) \tag{4}$$

Fig. 2 shows the fraction of the output voltage, $K_{ka}/|V_0|$, that diode D_1 must block as a function of the switching duty ratio (t_{on}/T), and the ratio of the transformer resetting time to the S switch *off* time (τ/t_{off}). If the switching duty ratio is, only, a few percent and the transformer resetting time extends to almost all the S switch off time, D_1 only blocks a small fraction of the output voltage. Moreover, with a step-up transformer, this topology enables also relatively low voltage semiconductor devices in the primary side, as in (2).

B. Step-up transformer

To assemble a demonstration level laboratory prototype, a step-up transformer with an available ETD49 core, with 3C85 grade material ferrite, from Philips, was designed for an output pulse of 5kV with 50 primary turns and 500 secondary turns and for 10kHz operating frequency with, roughly, 5μs pulse width. The transformer was specially built to minimize both capacitance and leakage inductance. First, to reduce parasitic capacitance double shielding was used. Second, the secondary was assembled in a staircase way to decrease leakage inductance.

To further reduce the transformer leakage inductance, two auxiliary windings, with the same number of turns, located as shown in Fig. 3, and connected in subtractive mode, have been added to the transformer, as suggested in [5].

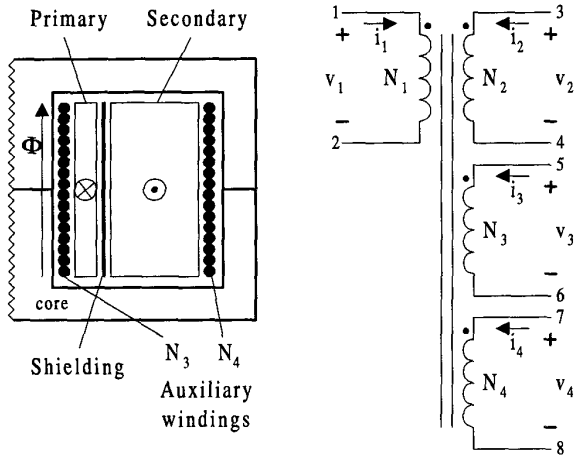

Fig. 3. Layout of the actual step-up transformer with the auxiliary windings, N_3 and N_4, and double shielding (left). Schematic representation of the theoretical step-up transformer with two auxiliary windings. Considering positive currents entering the windings through their positive (right).

Fig. 3 shows the schematic representation of the transformer. For this case, we consider that the system is linear and the winding capacitances are negligible. Let us consider positive currents entering the windings through their positive terminals, as is shown in Fig. 3, which results that each winding creates a flux with the same direction. Hence, the application of Faradays Law in each winding yields,

$$v_i = R_i i_i + \frac{d\psi_i}{dt} \tag{5}$$

where the subscript i is the index of each winding, v is the instantaneous terminal voltage, i is the instantaneous current, R is the effective resistance and ψ is the instantaneous flux linkage.

The flux in each winding has three components. First, the resultant flux, ϕ, that links all the windings produced by the currents i_1, i_2, i_3 and i_4. Second, the self-flux of each winding, ϕ_{ii}, produced by its individual current, i_i, that accounts for the leakage flux of each winding. Third, the mutual flux between pairs of windings, ϕ_{ij}, indicating the flux produced by current i_j that links, only, winding N_i. We can consider that second and third flux components are very nearly proportional to the currents producing them, since their paths are in air for a considerable portion of their lengths. So, in these cases we can introduce the self-inductance l_{ii} and the mutual inductance l_{ij}. Hence, the flux linkage in each winding is,

$$\varphi_1 = N_1\phi + l_{11}i_1 + l_{12}i_2 + l_{13}i_3 + l_{14}i_4 \tag{6}$$

$$\varphi_2 = N_2\phi + l_{21}i_1 + l_{22}i_2 + l_{23}i_3 + l_{24}i_4 \tag{7}$$

$$\varphi_3 = N_3\phi + l_{31}i_1 + l_{32}i_2 + l_{33}i_3 + l_{34}i_4 \tag{8}$$

$$\varphi_4 = N_4\phi + l_{41}i_1 + l_{42}i_2 + l_{43}i_3 + l_{44}i_4 \tag{9}$$

where, N_1, N_2, N_3 and N_4 represents the number of turns in each winding.

Now, lets consider the actual operating conditions of the transformer. The secondary winding is connected do load, Z_0, as in Fig. 1. Then $i_2=-i_0$, where i_0 is the load current. The auxiliary windings N_3 and N_4 are connected in subtractive mode. This means that in Fig. 3, terminal 5 is connected to terminal 7 and terminal 6 is connected to terminal 8. We consider that $i_3=-i_4$, where $i_4>0$. Calculating the instantaneous terminal voltages of winding N_3 and N_4 yields,

$$v_3 = -R_3 i_4 + N_3\frac{d\phi}{dt} + \\ + l_{31}\frac{di_1}{dt} - l_{32}\frac{di_0}{dt} - l_{33}\frac{di_4}{dt} + l_{34}\frac{di_4}{dt} \tag{10}$$

$$v_4 = +R_4 i_4 + N_4\frac{d\phi}{dt} + \\ + l_{41}\frac{di_1}{dt} - l_{42}\frac{di_0}{dt} - l_{43}\frac{di_4}{dt} + l_{44}\frac{di_4}{dt} \tag{11}$$

because $v_3=v_4$, the voltage equation of the connected auxiliary windings yields,

$$0 = R_{aux}i_{aux} + l_{aux}\frac{di_{aux}}{dt} - M_{aux}\frac{di_{aux}}{dt} + \\ + (l_{41} - l_{31})\frac{di_1}{dt} + (l_{32} - l_{42})\frac{di_0}{dt} \tag{12}$$

where, $R_{aux}= R_3+R_4$, $i_{aux}=-i_3=i_4$, $l_{aux}=l_{33}+l_{44}$, $M=l_{34}+l_{43}$. In addition, because $N_3=N_4$, in (12) there is no magnetizing component.

If we consider the auxiliary windings opened the voltages at their terminals are,

$$v_{30} = N_3\frac{d\phi}{dt} + l_{31}\frac{di_1}{dt} - l_{32}\frac{di_0}{dt} \tag{13}$$

$$v_{40} = N_4\frac{d\phi}{dt} + l_{41}\frac{di_1}{dt} - l_{42}\frac{di_0}{dt} \tag{14}$$

Due to the geometric position of the four windings in the transformer, let us consider the primary leakage flux linked preferentially with the third winding and the secondary

leakage flux linked preferentially with the fourth winding. This means that $l_{31}>>l_{41}$ and $l_{42}>>l_{41}$. Moreover, the magnetic coupling between the two auxiliary windings is neglected, $l_{34}=l_{43}=0$. Hence (12), (13) and (14) become, respectively,

$$l_{31}\frac{di_1}{dt}+l_{42}\frac{di_0}{dt}=R_{aux}i_{aux}+l_{aux}\frac{di_{aux}}{dt} \quad (15)$$

$$v_{30}=N_3\frac{d\phi}{dt}+l_{31}\frac{di_1}{dt} \quad (16)$$

$$v_{40}=N_4\frac{d\phi}{dt}-l_{42}\frac{di_0}{dt} \quad (17)$$

Excluding the theoretical hypothesis in (15) when $di_0/dt\neq 0$ and $di_1/dt\neq 0$ but $l_{31}di_1/dt+l_{42}di_0/dt=0$, we can consider three operation conditions, which originate a current, i_{aux}, across the auxiliary windings, when the primary, i_1, and/or load, i_0, currents vary. Considering Fig. 3, for $R_{aux}=0$,

1) $di_0/dt=0$ and $di_1/dt\neq 0$, $d_{iaux}/dt=(l_{31}/l_{aux})di_1/dt$.
The current i_{aux} across N_3 originates a flux that opposes the primary leakage flux;

2) $di_0/dt\neq 0$ and $di_1/dt=0$, $d_{iaux}/dt=(l_{42}/l_{aux})di_0/dt$.
The current i_{aux} across N_4 originates a flux that opposes the secondary leakage flux;

3) $di_0/dt\neq 0$ and $di_1/dt\neq 0$, $d_{iaux}/dt=(l_{31}/l_{aux})di_1/dt(l_{42}/l_{aux})di_0/dt$.
The current i_{aux} across N_3 and N_4 originates a flux that opposes the primary leakage flux and the secondary leakage flux, respectively.

In conclusion, we can say that the current, i_{aux}, is a function of the leakage flux coupling between the primary winding and N_3 and the secondary winding and N_4, generating a magnetic flux that only reduces the leakage flux of the primary and secondary windings. Consequently, the leakage inductance in the transformer is reduced. The resultant flux, ϕ, is not affected by the auxiliary windings.

III. Experimental Results and Discussion

The circuit in Fig. 1 was implemented with $R=600\Omega$, $C=4\mu F$ and a resistive load of $5k\Omega$. An 800V MOSFET, IXTH13N80, was used as the power switch and 1000V diode, BA159, for D_1 and D_2. For the auxiliary windings $N_3=N_4=25$ turns.

For $V_i=500V$, $(t_{on}/T)=5\%$, and $\Delta_1\approx 65\%$, Fig. 4 shows the output voltage, v_0, the primary voltage, v_1, the MOSFET gate voltage, v_{gs}, the primary, i_1, and load, i_0, currents, with the

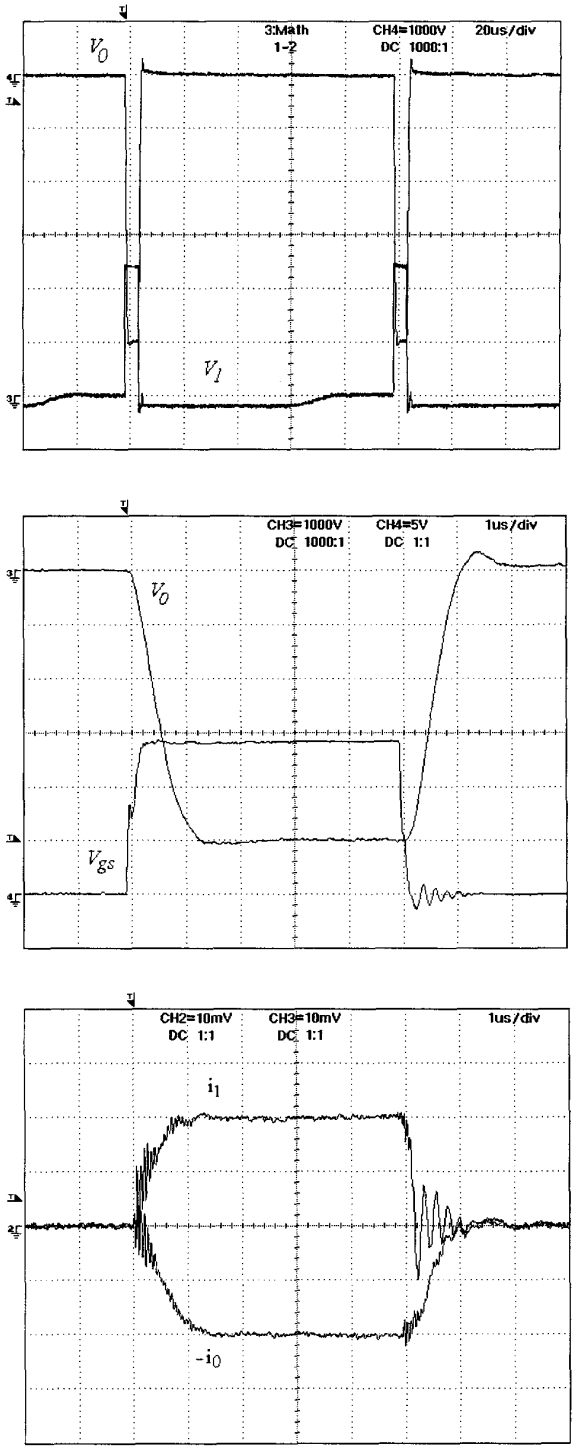

Fig. 4. With N_3 and N_4 open. For 20μs/div, v_0 (1000V/div) and v_1 (200V/div), top. For 1μs/div, v_0 (1000V/div) and v_{gs} (5V/div), middle. And i_1 (5A/div), $-i_0$ (0.5 A/div), bottom.

auxiliary windings open. An, almost, 5μs square pulse v_0 is obtained with –5kV and a rise time of, nearly, 0.8μs, Fig. 4.

Fig. 5 shows the comparison between the theoretical prediction for the ratio of the reverse voltage of diode, D_1, to the absolute value of the output voltage, $|V_0|$, based on (4) and on the experimental results for an input voltage of V_i=500V. A good agreement between (4) and the experimental values, is shown in Fig. 5, and for this case, with $D \approx 5\%$ and $(\tau/t_{off}) \approx 70\%$, the reverse voltage in diode D_1 is, approximately, 400V, about 8% of the output voltage V_0. This value is, also, taken from Fig. 4, times the turn's ratio.

Fig. 6 shows the open-circuit voltages of the auxiliary windings, v_{30} and v_{40} respectively. From (16) and (17), we can conclude that if the primary and secondary currents are constant the open-circuit voltages in N_3 and N_4 are proportional to the resultant flux, ϕ. With values equal, approximately to the turn's ratio, N_3/N_1 and N_4/N_1, times the primary voltage, 250V. This is, roughly, confirmed in Fig.6 during the time period where primary and load currents are stationary, as seen in Fig. 4. During the pulse rise and fall times, due to the difference in the number of turn's between N_1 and N_2 the value of l_{42} is greater than l_{31}.

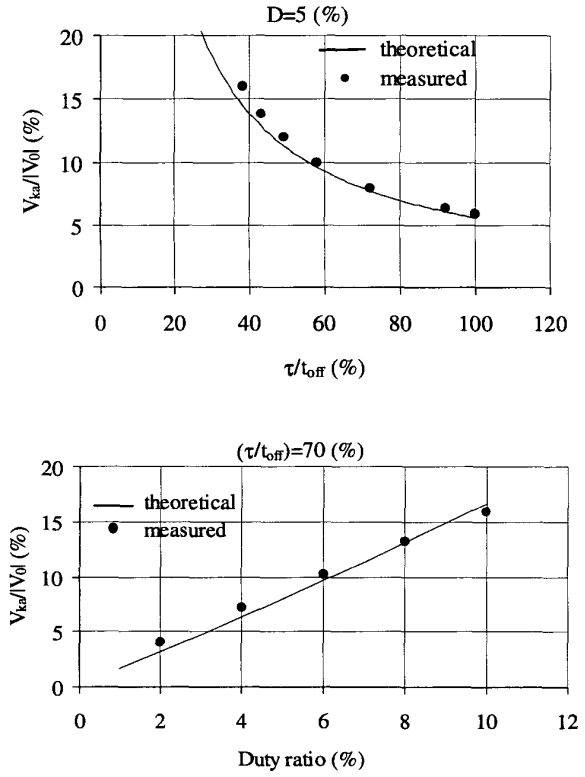

Fig. 5. Theoretical and experimental results for the value of the reverse voltage of diode D_1, taken for V_i=500V. As a function of the transformer resetting time to the switching off time (τ/t_{off}), with a constant duty ratio $D \approx 5\%$ (top). As a function of the duty ratio, D, with a constant transformer resetting time to the switching off time $(\tau/t_{off}) \approx 70\%$ (bottom).

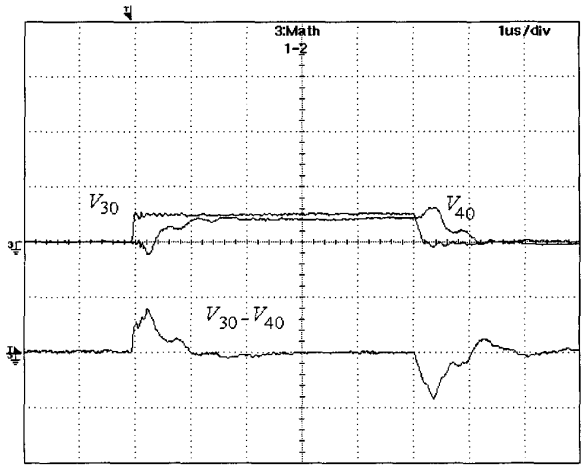

Fig. 6. The differentially measured open-circuit voltage v_{30} and v_{40} (500V/div). The differentially measured subtraction v_{30}-v_{40} (500V/div). Both for 1μs/div.

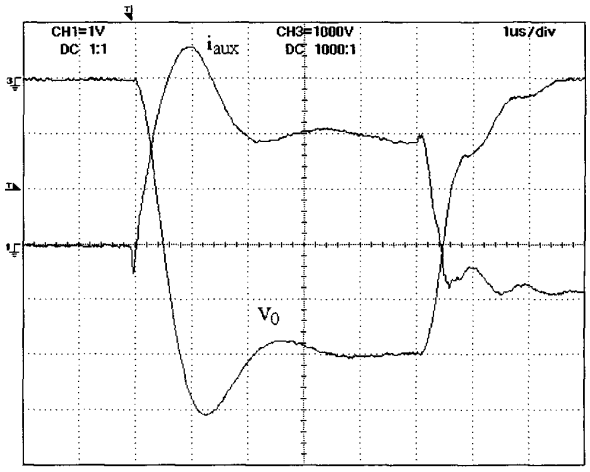

Fig. 7. With the auxiliary windings connected, i_{aux} (2A/div) and v_0 (1000V/div). Both for 1μV/div.

This means that the leakage component of (17), with direction opposite to the magnetizing component, has a much greater weight than the leakage component of (16), shown in Fig. 6. As can be seen from Fig. 4 the primary current, i_1, has a greater time derivative when compared with the load current, i_0, 10A/μs and 1A/μs, respectively. In spite of that fact v_{40} is much more deformed then v_{30} that has the expected shape due to the magnetizing component. Fig. 6, also, shows the subtraction between v_{30} and v_{40}, which is taken connecting the positive terminals of N_3 and N_4 and measuring the voltage between the other two terminals. The result is well understood, since from (16) and (17),

$$v_{30} - v_{40} = l_{31}\frac{di_1}{dt} + l_{42}\frac{di_0}{dt} \tag{18}$$

which is zero when the currents are stationary.

Fig. 7 shows the current, i_{aux}, in the auxiliary windings, when connected. The time evolution of this current is ruled by (15). At the beginning of the pulse there is a fast rising current in the auxiliary windings that generates a magnetic flux, which opposes to the leakage flux of the primary and secondary windings. The same, but with opposite sign, happens at the end of the pulse. In between, the time derivatives of i_1 and i_0 are zero, and the auxiliary current would fall slowly to zero.

The resultant output voltage, v_0, when the auxiliary windings are connected, as shown in Fig. 7, exhibit a 25% (200ns) decrease in the pulse rise time (600ns). To reduce the 20% overshoot originated from the auxiliary winding, an auxiliary switch was introduced in order to open the auxiliary windings just before the output voltage reaches the desire value. To control this switching process a current transducer was introduced in the auxiliary winding circuit connected to a hysteresis comparator, as shown in Fig. 8. The auxiliary windings are opened for, approximately, 1.2μs resulting in a smoother output pulse, v_0, as shown in Fig. 9. After that they are connected again.

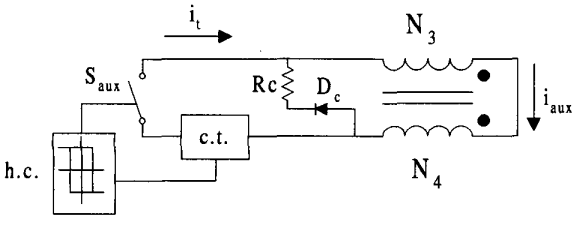

Fig. 8. Simplified diagram of the controlled switch of the auxiliary winding circuit. Auxiliary switch (S_{aux}), current transducer (c.t.), hysteresis comparator (h.c.), freewheeling diode, D_c, and resistance R_c.

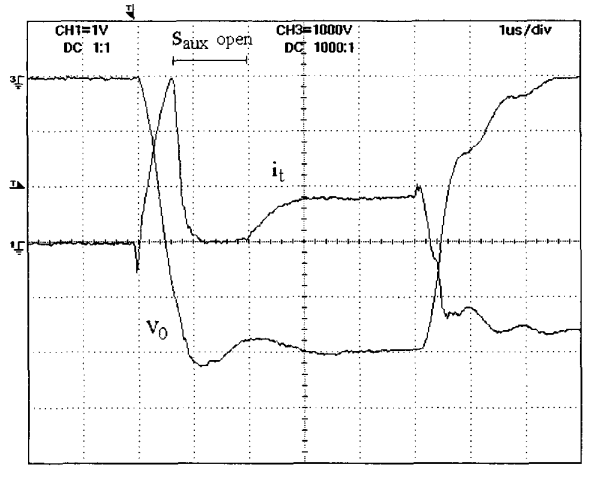

Fig. 9. Controlled switching of the auxiliary winding circuit. Output voltage v_0 (1000V/div), and transducer current i_t (2A/div), for (1μs/div).

IV. Conclusions

A new method to reduce voltage stress on all semiconductor switches of kV pulsed supplies has been proposed. The reverse voltage of the diode placed in the secondary of a step-up transformer was determined theoretically, as a small fraction of the output voltage, v_0, and experimentally verified. The pulse rise time improvement introduced by the auxiliary winding, to reduce transformer leakage flux, was studied and experimentally confirmed. A 25% decrease in the output voltage rise time was obtained. To reduce the voltage overshoot caused by the auxiliary winding, controlled switching of this winding was tested. Today, with 4.5kV IGBTs and 3.3kV diodes, a 30kV high voltage pulse power supply using this concept can be built. Higher voltages can be foreseen by cascading the secondary windings of two transformers.

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