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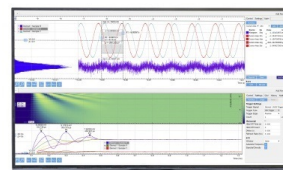
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## ABSTRACT

Silicon quantum dot spin qubits have great potential for application in large-scale quantum circuits as they share many similarities with conventional transistors that represent the prototypical example for scalable electronic platforms. However, for quantum dot formation and control, additional gates are required, which add to device complexity and, thus, hinder upscaling. Here, we meet this challenge by demonstrating the scalable integration of a multilayer gate stack in silicon quantum dot devices using self-alignment, which allows for ultra-small gate lengths and intrinsically perfect layer-to-layer alignment. We explore the prospects of these devices as hosts for hole spin qubits that benefit from electrically driven spin control via spin-orbit interaction. Therefore, we study hole transport through a double quantum dot and observe current rectification due to the Pauli spin blockade. The application of a small magnetic field leads to lifting of the spin blockade and reveals the presence of spin-orbit interaction. From the magnitude of a singlet-triplet anticrossing at a high magnetic field, we estimate a spin-orbit energy of  $\sim 37\mu\text{eV}$ , which corresponds to a spin-orbit length of  $\sim 48\text{ nm}$ . This work paves the way for scalable spin-based quantum circuits with fast, all-electrical qubit control.

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Classical computers are made of silicon (Si) integrated circuits that consist of billions of fully operational metal-oxide-semiconductor field-effect transistors (MOSFETs). Their quantum analog is represented by Si-MOS quantum dots,<sup>1,2</sup> which, in their role as hosts for coherent and high-fidelity spin qubits,<sup>3–11</sup> are among the prime candidates for implementing large-scale quantum processors.<sup>12–14</sup> While MOSFETs work with three terminals (source, drain, and gate), a multilayer gate stack is often required for quantum dot devices.<sup>1,2,5–9,15,16</sup> Consequently, tight requirements on the feature size and layer-to-layer alignment make quantum dot fabrication highly demanding. Furthermore, the high gate count leads to challenges in wiring up of large-scale qubit systems.<sup>12,13</sup> It is, therefore, too simplistic to assume that Si spin qubits based on industrial manufacturing processes are *a priori* scalable. Yet, the current quantum dot device fabrication standards need to be adapted for scalable integration.

In the Si industry, self-alignment techniques are used to reduce feature sizes and to overcome alignment limitations. Here, the key idea is to make use of an existing patterned structure on a device to define

the pattern of a subsequent process, resulting in an intrinsically perfect layer-to-layer alignment. A prime example from the electronics industry is to employ the gate of a MOSFET as a mask for the definition of source and drain regions by means of ion implantation.<sup>17,18</sup> This led to a large increase in computer performance in the 1970s.

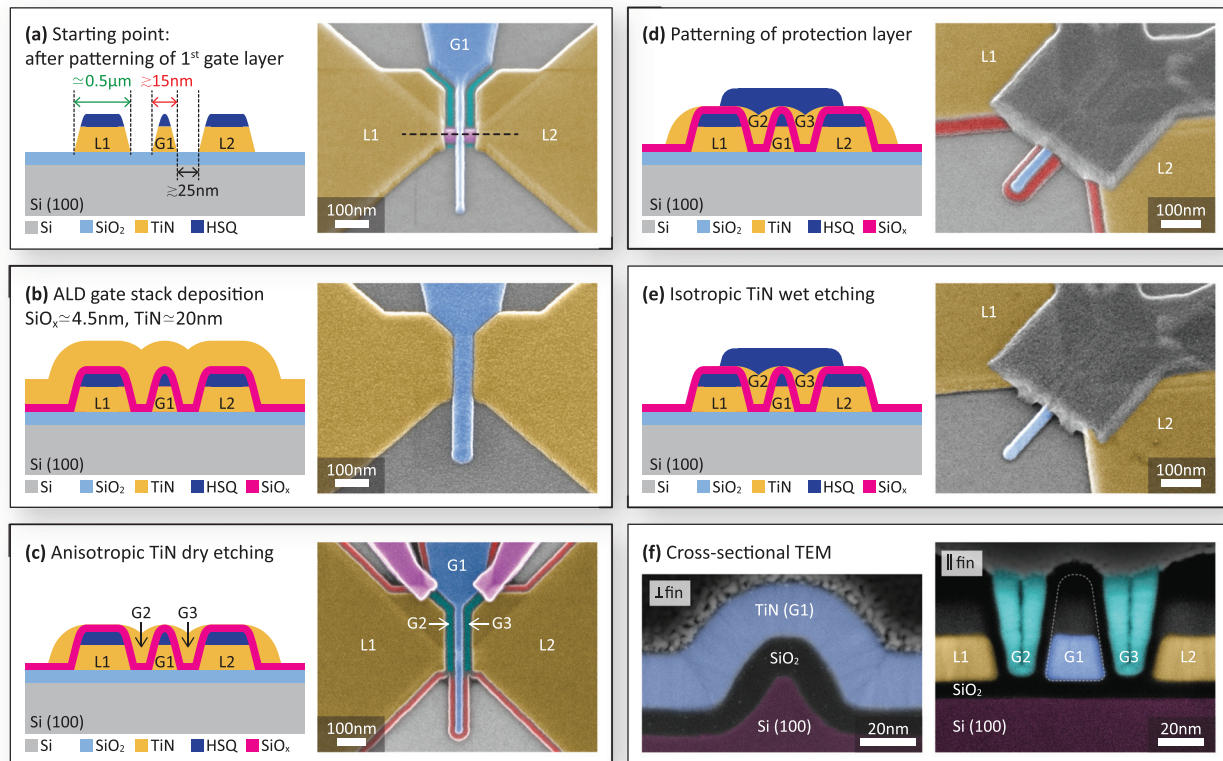
In order to limit device complexity and qubit crosstalk in large-scale quantum dot arrays, all-electrical spin control is to be preferred over magnetic field control. Unlike electron spin qubits in Si,<sup>5–10</sup> their hole counterparts<sup>11,19,20</sup> are subject to a strong spin-orbit interaction (SOI), facilitating fast, all-electrical spin control.<sup>11,21</sup> In contrast, electron spin manipulation is driven by magnetic fields, requiring additional device components such as a magnetic field creating transmission line<sup>5,6</sup> or micromagnet,<sup>7,22</sup> which increase device complexity. Furthermore, an exceptionally strong and electrically tunable SOI has been predicted for holes in Si nanowires.<sup>23,24</sup> This will allow for on-demand switching between qubit idling (low SOI) and fast manipulation (high SOI) modes by changing an electric field.

In this work, we demonstrate scalable integration of a multilayer gate stack with Si quantum dot devices, which are fabricated by employing a bulk fin field-effect transistor process.<sup>11,25</sup> We implement hole double quantum dots by using self-alignment of a second gate layer, where the first gate layer serves as a mask for the following one. This process achieves ultra-small gate lengths and perfect layer-to-layer alignment. We investigate hole transport in the Pauli spin blockade (PSB) regime and identify SOI as the dominant spin blockade lifting mechanism. Both the SOI energy and the effective hole  $g$ -factor are extracted from an avoided crossing between singlet and triplet spin states at a high magnetic field.

Integration of the self-aligned second gate layer follows processing of the Si fin and the first gate level. These preceding fabrication steps are described in detail elsewhere.<sup>25</sup> In Fig. 1(a), a scanning electron microscope (SEM) image of a device at this fabrication stage is shown. The first gate layer consists of a central nanoscale finger gate (G1) and two individual lead gates (L1 and L2) for source and drain reservoirs. The gaps that separate these gates create channels

[turquoise highlights in Fig. 1(a)], which serve as a template for the second gate layer. By means of plasma-enhanced atomic layer deposition at 300 °C, the gate material stack, consisting of  $\approx 4.5$  nm silicon oxide ( $\text{SiO}_x$ , 3DMAS precursor, and  $\text{O}_2$  plasma) and  $\approx 20$  nm metallic titanium nitride (TiN, TDMAT precursor, and  $\text{N}_2/\text{H}_2$  plasma), is deposited with highly uniform surface coverage [see Fig. 1(b)]. Provided that the width of the gaps separating G1 from L1 and L2 is less than twice the thickness of the deposited material, the channels are almost evenly filled. The thin  $\text{SiO}_x$  layer ensures a good electrical isolation of the two gate layers (breakdown voltage  $\geq 6$  V, see the supplementary material, S1).

Next, an anisotropic TiN dry etch (inductively coupled HBR plasma) is applied for a duration that corresponds to the deposited metal thickness of  $\approx 20$  nm [see Fig. 1(c)]. While TiN is removed during etching from the flat surfaces of the device, leftovers are found at the topography steps. The metal residues inside the predefined channels naturally form gates G2 and G3 of the second gate layer. The gate fan-out to microscale contact pads is protected during etching by a



**FIG. 1.** Fabrication process flow. [(a)–(e), left panel] Schematic of the device cross section along the black dashed line of the (a) SEM image. The horizontal axes of the left and right panels are scaled differently. (a) Device with a completed first gate layer, consisting of two lead gates L1 and L2 (yellow in SEM image) and a central finger gate G1 (blue) that is wrapped around the Si fin (magenta). EBL with hydrogen silsesquioxane (HSQ) resist is employed for gate definition. The gaps separating the gates (turquoise) act as a template for the second gate layer. (b) Deposition of the gate stack by means of ALD results in a uniform surface coverage, such that the gaps are almost evenly filled with material. (c) TiN is removed from the flat surfaces, which are not protected by resist (magenta), by timed dry etching. TiN residues (red) at topography steps still connect gates G2 and G3 of the second gate layer. (d) and (e) A protective resist mask is applied to remove all unintended TiN residues with an isotropic wet etch. (f) Cross-sectional TEM images perpendicular (left panel) and parallel (right panel) to the fin. Left: the quantum dot is induced at the apex of the roughly triangular-shaped Si fin (purple). Right: Gates G2 and G3 (turquoise) are perfectly aligned relative to the first gate layer. Good electrical isolation is ensured by a thin  $\text{SiO}_x$  layer sandwiched between the two gate layers.

resist mask [magenta highlights in Fig. 1(c)], which is defined by electron-beam lithography (EBL). The demands of this lithography step with regard to resolution and alignment accuracy are lowered by moving the channel end points further away from the fin center.

At this stage, gates G2 and G3 are still connected via the TiN that remains and is highlighted in red in Figs. 1(c) and 1(d). This short circuit is eliminated by first protecting the gates with a resist mask [Fig. 1(d)] and then by selectively removing all the unintentional TiN residues by isotropic wet etching [Fig. 1(e)]. The protective cover is defined by means of EBL.

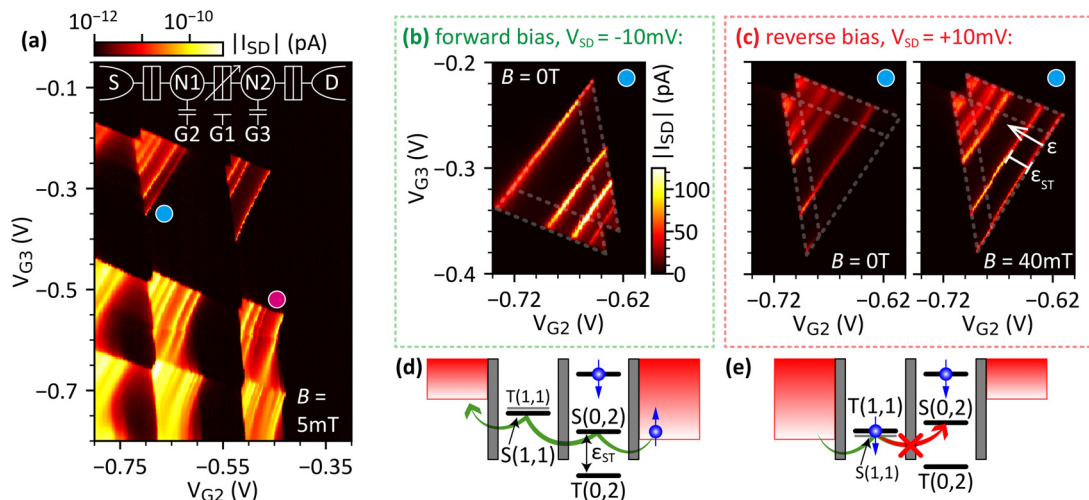
After successful integration of the second gate layer, cross-sectional transmission electron microscope (TEM) images along and perpendicular to the fin direction are taken [Fig. 1(f)]. These images confirm ultra-small gate lengths and perfect layer-to-layer alignment. All the remaining fabrication steps, leading to a fully operational device, are described elsewhere.<sup>25</sup>

The device layout with the three nanoscale gates G1, G2, and G3 allows for both a single- and double-dot operation mode. The latter one is explored in this work for *p*-type devices (see the supplementary material, S2 for single-dot operation). Holes are accumulated in source and drain reservoirs through platinum silicide contacts, by a strong negative lead gate voltage ( $V_{L1,L2} = -4.5$  V). Gates G2 and G3 form quantum dots 1 and 2 and control their occupancy (see the inset of Fig. 2(a) for a simplified equivalent circuit of the device). Gate G1, which is sandwiched between G2 and G3, is used to control the inter-dot tunnel coupling (see the supplementary material, S3). The gate lengths of the device used here are  $\approx 25$  nm for the inter-dot barrier gate and  $\approx 15$  nm for the plunger gates.

The data presented here are obtained from direct current electrical transport measurements with the sample cooled to 0.55 K. In Fig. 2(a), a double dot charge stability diagram, showing the first observable pairs of bias triangles, is presented<sup>26</sup> (see the supplementary

material, S4 for the same measurement on a similar device). The two triangles of each pair strongly overlap for a source-drain voltage of  $V_{SD} = +10$  mV. While the lines of strong current flow parallel to the triangle base reveal elastic tunneling between the ground or excited states of the double dot, the background current inside the triangles can be assigned to inelastic tunneling.<sup>26</sup> The triangles for more negative gate voltages are distorted by co-tunneling processes because of the dots' increased tunnel coupling to the reservoirs.<sup>27,28</sup>

In Figs. 2(b) and 2(c), a zoom-in on the pair of bias triangles, indicated by a solid blue circle in Fig. 2(a), is presented for negative and positive  $V_{SD}$ . While current flow through the base of the triangles is observed for  $V_{SD} = -10$  mV, it is strongly suppressed for positive  $V_{SD}$  at zero magnetic field  $B$ . (For the bias triangles marked by a solid magenta circle in Fig. 2(a), current suppression is observed for the opposite bias direction, see the supplementary material, S5). This type of current rectification is a hallmark of PSB<sup>29–33</sup> and is due to spin-conserved tunneling, as schematically depicted in Figs. 2(d) and 2(e). If two hole spins reside on the same dot (here the right one), they must occupy a spin singlet state  $S(0, 2)$  as the triplet state  $T(0, 2)$  is shifted to higher energy by the single-dot singlet-triplet splitting  $\epsilon_{ST}$ .<sup>31</sup> Here, a pseudospin of  $\pm 1/2$  is assigned to each hole spin,<sup>34</sup> and  $(m, n)$  denotes the effective hole occupancy of the left and right quantum dot. While our data are consistent with observing the last hole, more sensitive charge detection methods are required to evaluate this.<sup>31,35</sup> For a negative  $V_{SD}$ , charge transport occurs from the  $S(0, 2)$  state to the  $S(1, 1)$  state, and a hole can escape the left dot to the reservoir. In contrast, for a positive  $V_{SD}$ , current flow is blocked. If one hole spin resides on each dot, they can form either a  $S(1, 1)$  or  $T(1, 1)$  state, which are nearly degenerate in energy for weak inter-dot coupling. Once the  $T(1, 1)$  state is occupied by loading a hole from the reservoir to the left dot, transport is blocked by spin conservation during tunneling.

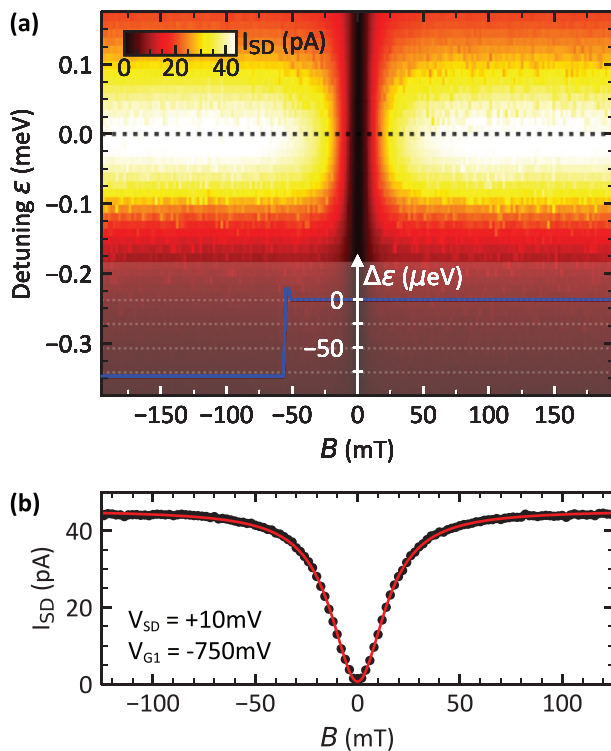


**FIG. 2.** Bias triangles and Pauli spin blockade for holes. (a) Double dot charge stability diagram measured for  $V_{SD} = +10$  mV and  $V_{G1} = -770$  mV. The simplified equivalent circuit of the device is depicted in the inset. While the dot occupancies N1 and N2 are separately controlled by gates G2 and G3, the inter-dot tunnel barrier is tuned by G1. The colored circles mark the pairs of bias triangles for which signatures of PSB are observed. A close-up of the triangles indicated by the solid blue circle in (a) is presented for  $V_{G1} = -750$  mV, in (b) for  $V_{SD} = -10$  mV, and in (c) for  $V_{SD} = +10$  mV. While for negative  $V_{SD}$ , current can freely flow through the base of the triangles, it is blocked for positive  $V_{SD}$  at zero magnetic field. PSB is lifted for a detuning  $\epsilon \geq \epsilon_{ST}$  or by applying a small magnetic field, here  $B = 40$  mT. The detuning axis is defined as indicated by the white arrow. A charge transport cycle is depicted schematically in (d) for negative and (e) for positive  $V_{SD}$ .

PSB is lifted for an inter-dot energy level detuning  $\epsilon$  exceeding  $\epsilon_{ST}$  since the  $T(0, 2)$  state becomes accessible from the  $T(1, 1)$  state. Hence, the reappearance of current along the detuning axis determines  $\epsilon_{ST} \simeq 1.85$  meV. This allows us to give an upper-bound estimate of the effective dot size  $\lambda_x \sim \hbar/\sqrt{m^* \epsilon_{ST}} = 9.5$  nm,<sup>36</sup> which is in good agreement with the device geometry. Here, we assume harmonic confinement and an effective hole mass of  $m^* = 0.45 m_0$ , where  $m_0$  denotes the bare electron mass.<sup>23</sup>

For  $\epsilon < \epsilon_{ST}$ , spin relaxation leads to a leakage current through the spin-blocked region of the bias triangles.<sup>37–40</sup> For a small magnetic field of  $B = 40$  mT (magnetic fields are applied out-of-plane), current leaks through the base of the triangles [see Fig. 2(c)]. For  $B \neq 0$ , the previously forbidden  $T(1, 1) \rightarrow S(0, 2)$  transition becomes allowed because hole spins in Si experience a strong SOI<sup>23</sup> that hybridizes the  $T(1, 1)$  and  $S(0, 2)$  states.<sup>39,40</sup>

The leakage current dependence on  $B$  and  $\epsilon$  for positive  $V_{SD}$  is shown in Fig. 3(a). A dip in the leakage current, which is centered around zero magnetic field, is revealed by a linecut along  $B$  at  $\epsilon = 0$  in Fig. 3(b). This dip has a Lorentzian line shape with a full-width at half-maximum (FWHM) of 32 mT and a close-to-zero minimum value, signifying a very efficient spin blockade. The dip also confirms that



**FIG. 3.** Spin blockade leakage current. (a) Source-drain current  $I_{SD}$  under reverse bias as a function of detuning  $\epsilon$  and out-of-plane magnetic field  $B$ . Some of the vertical traces are shifted along the  $\epsilon$ -axis to eliminate the random switching of a charge trap. The detuning correction  $\Delta\epsilon$  is plotted in the inset and uncovers one single switching event for the measurement. (b) Cut along  $B$  at  $\epsilon = 0$ , as indicated by the black dashed line in (a). The data (black dots) are well fitted by a Lorentzian function (red curve) of FWHM = 32 mT.

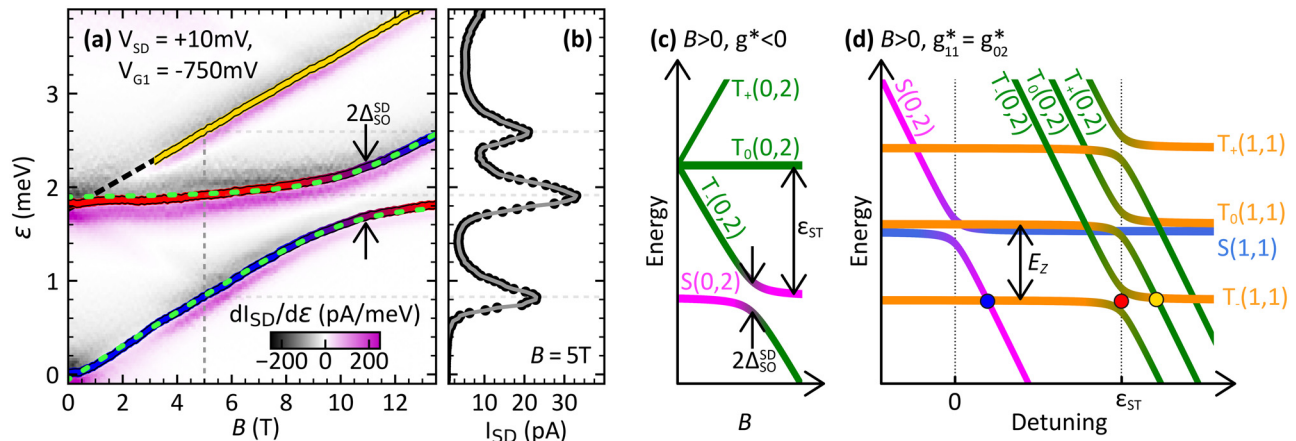
lifting of PSB is dominated by SOI,<sup>33,39</sup> since hyperfine interactions<sup>37,40</sup> or spin-flip cotunneling<sup>32,41,42</sup> yield a zero-field peak.

An extension of Fig. 3(a) to larger magnetic fields and detunings, revealing SOI-mediated singlet-triplet mixing, is shown in Fig. 4(a). Resonant charge transport takes place for detunings, where  $(1, 1)$  and  $(0, 2)$  states are degenerate in energy and hybridized by a finite coupling [Fig. 4(d)]. Due to a low level of charge noise, no detuning correction had to be applied to the data.<sup>33</sup> As shown in Fig. 4(b), three current peaks are observed within the  $\epsilon$  range of Fig. 4(a), showing the  $B$ -dependence of the peak center positions. For a weak tunnel coupling and a negative effective hole  $g$ -factor  $g^*$ , the bottom two curves in Fig. 4(a) can be assigned to the  $T_-(1, 1) \rightarrow S(0, 2)$  and  $T_-(1, 1) \rightarrow T_-(0, 2)$  transitions.<sup>33</sup> Thus, the  $T_-(1, 1)$  state can be utilized to probe the energy splitting of the  $S(0, 2)$  and  $T_-(0, 2)$  states [Fig. 4(c)].

While the central red curve remains almost constant in  $\epsilon$  for  $B \lesssim 3$  T, indicating a spin-conserving transition, the bottom curve shifts by the Zeeman energy  $E_Z = g_{11}^* \mu_B B$ , where  $g_{11}^*$  denotes the effective hole  $g$ -factor for  $T_{\pm}(1, 1)$  and  $\mu_B$  the Bohr magneton. From the line slope, we, thus, obtain  $|g_{11}^*| = 3.2 \pm 0.3$ , a value similar to those reported before.<sup>21,33</sup> The small initial slope of the red transition reveals a  $g^*$ -factor difference between the  $(1, 1)$  and  $(0, 2)$  triplet states of  $\simeq 0.2$ . When  $g_{02}^* \mu_B B$  approaches  $\epsilon_{ST}$ , the  $S(0, 2)$  and  $T_-(0, 2)$  states first begin to align in energy but then anticross due to the SOI [Fig. 4(c)].<sup>36</sup> This level repulsion causes the avoided crossing of the two bottom curves in Fig. 4(a) at  $B \simeq 10.9$  T. From the magnitude of the anticrossing, we can obtain the single-dot spin-orbit gap  $\Delta_{SO}^{SD} = 0.27 \pm 0.03$  meV. The spin-orbit length is estimated to be  $\lambda_{SO} \sim \epsilon_{ST} \lambda_x / (\sqrt{2} \Delta_{SO}^{SD}) = 48$  nm,<sup>36,43</sup> which is roughly half the value reported for holes in planar Si quantum dot structures.<sup>33</sup> The spin-orbit energy is related to  $\lambda_{SO}$  by  $E_{SO} \sim \hbar^2 / (2m^* \lambda_{SO}^2) = 37$   $\mu$ eV, a value in very good agreement with theoretical predictions.<sup>23</sup> Using  $\epsilon_{ST} = 1.85$  meV in addition to the parameters mentioned before, we can overlay our data with the standard expression for two-level repulsion<sup>36</sup> [green curves in Fig. 4(a)] and find good agreement.

To summarize, we introduced a self-aligned second gate layer to spin qubit fabrication in Si fin field-effect transistors. This allows us to reduce the gate pitch and to enhance both the tunability and the stability of the devices. We demonstrate reproducible formation of low-disorder Si double quantum dots and investigate spin-dependent hole transport. From the observation of PSB, we obtain a single-dot singlet-triplet splitting of  $\epsilon_{ST} \simeq 1.85$  meV, indicating large orbital energies due to ultra-small gate lengths. The magnetic field dependence of the leakage current identifies SOI as the dominant spin blockade lifting mechanism. An effective hole  $g$ -factor of  $|g^*| = 3.2$  and a single-dot spin-orbit gap of  $\Delta_{SO}^{SD} = 0.27$  meV, which corresponds to a spin-orbit energy of  $E_{SO} \sim 37$   $\mu$ eV, are determined by modeling a two-level anti-crossing occurring at  $B = 10.9$  T. These results demonstrate that hole spins in Si are promising candidates for building a scalable network of small, fast, and electrically controllable qubits.

Self-aligned gate layers have great potential for application in integrating spin-based multi-qubit devices. This fabrication methodology is very general and can easily be applied to other quantum dot qubit platforms, such as planar Si-MOS structures<sup>1,2,5–7</sup> or Si/Si-germanium heterostructures.<sup>8–10</sup> For holes in Si nanowires or fin field-effect transistors, qubit performance can further be enhanced toward an ultra-strong and electrically switchable SOI by optimizing the device geometry.<sup>23,24</sup>



**FIG. 4.** Spin state mixing by SOI. (a) Detuning energy of the three observed resonant current peaks as a function of magnetic field. The peak positions are extracted from current traces, such as the one presented in (b) for  $B = 5$  T. The differentiated data  $dI_{SD}/d\epsilon$  are shown in the background. The anticrossing of the two bottom curves is fitted with the standard expression for two-level repulsion (green dashed curves). For  $B \leq 3$  T, the energy splitting of the top and central peak cannot be resolved. (c) Magnetic field dependence of the double dot energy levels for the  $(0, 2)$  charge configuration. The degeneracy of the triplet spin states  $T_{+}$ ,  $T_0$ , and  $T_{-}$  is lifted by the Zeeman splitting  $E_Z$ . For  $E_Z = \epsilon_{ST}$ , the  $S(0, 2)$  and  $T_{-}(0, 2)$  states hybridize due to SOI and anticross. (d) Double dot energy diagram vs detuning at a finite magnetic field. Spin-conserved tunneling induces avoided crossings between states that share the same spin polarization.<sup>31</sup> The blue, red, and yellow dots mark the transitions denoted with the same colors in (a).

See the [supplementary material](#) for breakdown voltage of the  $\text{SiO}_x$  layer, single-dot operation mode, tunability of the inter-dot tunnel coupling, charge stability diagram of a second device, and PSB measurement at other charge transition.

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## DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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